

6/3/2025

DATE



REQUIRED COURSE



ELECTIVE COURSE

TEC DIVISION

 NEW COURSE REVISION

Lake Land College

Course Information Form

COURSE NUMBER:	EET-048	TITLE: (30 Characters Max)	Digital Circuits						
SEM CR HRS:	3.0	Lecture:	2.0	Lab:	2.0	ICCB Lab:	2.0	ECH:	4.0
Course Level:	<input type="checkbox"/> Gen Ed/IAI <input checked="" type="checkbox"/> Career/Technical <input type="checkbox"/> Baccalaureate/Non-IAI <input type="checkbox"/> Dev Ed/Not in Degree Audit			Clinical Practicum:	0.0	Work-based Learning:	0.0	WBL ECH:	0.0
Course PCS & CIP:	12 - 15.0303		IAI Code:	N/A			Contact Hours (Minutes/Week)		
Repeatable (Y/N):	N	Pass/Fail (Y/N):	N	Variable Credit (Y/N):		Min:		Max:	
						16 Wks	200	8 Wks	400
Prerequisites:	EET-076								
Corequisites:	None								
Catalog Description: (40 Word Limit)	Applications of digital circuits and devices to consumer products. Advanced application or digital logic fundamentals in design operation of digital circuits and systems.								

List the Major Course Segments (Units)	Contact Lecture Hours	Contact Lab Hours	Clinical Practicum	Work-based Learning
Registers	6	4		
Counters	6	10		
CPU	12	16		
Decoders, encoders, multiplexers and demultiplexers	3			
TTL, CMOS logic families	3			
TOTAL	30	30	0	0

EVALUATION

QUIZZES <input checked="" type="checkbox"/>	EXAMS <input checked="" type="checkbox"/>	ORAL PRES <input type="checkbox"/>	PAPERS <input type="checkbox"/>
LAB WORK <input checked="" type="checkbox"/>	PROJECTS <input type="checkbox"/>	COMP FINAL <input checked="" type="checkbox"/>	OTHER <input type="checkbox"/>

COURSE MATERIALS

TITLE: Digital Electronics	
AUTHOR: Tokheim	
PUBLISHER: McGraw Hill	
VOLUME/EDITION/URL: 7th edition	
COPYRIGHT DATE: 2008	

MAJOR COURSE SEGMENT	HOURS	LEARNING OUTCOMES
		<i>The student will be able to:</i>
Registers	10	1. Understand shift registers, serial and parallel data transfer. 2. Construct and test a 7-segment display circuit. 3. Construct and test NAND and NOR gate flip-flop.

Counters	16	<ol style="list-style-type: none"> 1. Demonstrate how asynchronous (ripple) binary counters work and that counters use unconventional signal flow. 2. Describe mod number and state transition diagrams. 3. Use counters to decode BCD. 4. Cascade counters to count in BCD. 5. Understand when Schmitt trigger devices might be needed. 6. Design and simulate a 4-bit binary counter (74LS93). 7. Design and simulate a 60-counter using both a decade counter and a binary counter. 8. Explore the differences between re-triggerable and non-retriggerable one-shots.
CPU	28	<ol style="list-style-type: none"> 1. Demonstrate basic microprocessor principles and digital logic programming to include ALU, buses, program counters and memory. 2. Design and simulate a working microprocessor circuit.
Decoders, encoders, multiplexers and demultiplexers	3	<ol style="list-style-type: none"> 1. Explain decoders, encoders, multiplexers and demultiplexers and binary to BCD.
TTL, CMOS logic families	3	<ol style="list-style-type: none"> 1. Cite the basic characteristics of digital ICs. 2. Differentiate TTL and CMOS. 3. Design and simulate a working alarm clock complete with snooze alarm. 4. Design and simulate a working CPU with display options.
	60	

Outcomes*	Outcome Title	At the successful completion of this course, students will be able to:
Course Outcome 1	Operate 7-segm Decod	Demonstrate the operation of a 7-segment decoder.
Course Outcome 2	Circuit InOutput Log	Design and construct counter logic circuits and describe the circuits' input/output logic.
Course Outcome 3	Combinat Log Circuit	Troubleshoot combinatorial logic circuits.
Course Outcome 4	Programmable Counter	Design and construct a programmable counter.
Primary Laker Learning Competency	Critical Thinking: Students connect knowledge from various disciplines to formulate logical conclusions.	
Secondary Laker Learning Competency	Scientific Literacy: Students apply the scientific process to real-life situations.	

*Course and program outcomes will be used in the software for outcomes assessment and should include at least 1 primary and 1 secondary Laker Learning Competency. Limit to 3-5.